CLAIM LISTING

1. (Currently Amended) A method for displaying progressive frames, said method comprising:

displaying a first portion of a progressive frame; and

writing a second portion of the progressive frame while displaying the first portion of the progressive frame.

2. (Currently Amended) The method of claim 1, wherein writing the second portion of the progressive frame further comprises:

overwriting a third portion of the progressive frame with the second portion of the progressive frame.

3. (Currently Amended) The method of claim 1, wherein writing the second portion of the progressive frame further comprises:

decoding the second portion of the progressive frame.

4. (Currently Amended) The method of claim 1, further comprising:

displaying the second portion of the progressive frame responsive to displaying the first portion of the progressive frame;

overwriting the first portion of the progressive frame with a fourth portion of the progressive frame.

5. (Currently Amended) The method of claim 1, further comprising:

displaying the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

overwriting the first portion of the progressive frame with a first portion of another progressive frame while displaying the second portion of the progressive frame.

6. (Currently Amended) The method of claim 1, wherein the progressive frame comprises a high definition television progressive frame.

7. (Currently Amended) A circuit for displaying progressive frames, said circuit comprising:

a memory for storing a first portion of a progressive frame;

a display engine for displaying the first portion of the progressive frame; and

a controller for writing a second portion of the progressive frame in the memory, while the display engine displays the first portion.

8. (Currently Amended) The circuit of claim 7, wherein the controller overwrites a third portion of the progressive frame with the second portion of the progressive frame in the memory.

9. (Currently Amended) The circuit of claim 7, wherein the controller decodes the second portion of the progressive frame.

10. (Currently Amended) The circuit of claim 7, wherein:

the display engine displays the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

the controller overwrites the first portion of the progressive frame with a fourth portion of the progressive frame in the memory.

11. (Currently Amended) The circuit of claim 7, wherein:

the display engine displays the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

the controller overwrites the first portion of the progressive frame with a first portion of another progressive frame while the display engine displays the second portion of the progressive frame.

12. (Currently Amended) The circuit of claim 7, wherein the memory further comprises:

a first prediction frame buffer for storing a first prediction frame;

a second prediction frame buffer for storing a second prediction frame; and

a delta frame buffer for storing the first portion of the progressive frame and the second portion of the progressive frame.

13. (Currently Amended) The circuit of claim [13] 12, wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive

frame comprise high definition television progressive frames with at least 1280x720 resolution.

14. (Currently Amended) The circuit of claim 13, wherein the memory comprises no more than 8 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1920x1080 resolution.

15. (Currently Amended) An integrated circuit for storing decoded frames, said integrate circuit comprising:

a first prediction frame buffer for storing a first progressive frame;

a second prediction frame buffer for storing a second progressive frame; and

a delta frame buffer for storing a portion of a third progressive frame.

16. (Currently Amended) The integrated circuit of claim 15, wherein the integrated circuit comprises no more than 4 megabytes of memory, and wherein the first progressive frame and the second progressive frame and the third progressive frame comprise high definition television frames with at least 1280x720 resolution.

17. (Currently Amended) The integrated circuit of claim 15, wherein the integrated circuit comprises no more than 8 megabytes of memory, and wherein the first progressive frame and the second progressive frame and the

third progressive frame comprise high definition television frames with at least 1920x1080 resolution.

Please add the following new claims

--18. (New) A circuit for displaying interlaced frames, said circuit comprising:

a memory for storing a first portion of a field;

a display engine for displaying the first portion of the field; and

a controller for writing a second portion of the field in the memory, while the display engine displays the first portion of the field.

19. (New) The circuit of claim 18, wherein the controller overwrites a third portion of the field with the second portion of the field in the memory.

20. (New) The circuit of claim 18, wherein the controller decodes the second portion of the field.

21. (New) The circuit of claim 18, wherein:

the display engine displays the second portion of the field responsive to displaying the first portion of the field; and

the controller overwrites the first portion of the field with a fourth portion of the field in the memory.

22. (New) The circuit of claim 18, wherein:

the display engine displays the second portion of the field responsive to displaying the first portion of the field; and

the controller overwrites the first portion of the field with a first portion of another field while the display engine displays the second portion of the field.

23. (New) The circuit of claim 18, wherein the memory further comprises:

a first prediction frame buffer for storing a first prediction frame;

a second prediction frame buffer for storing a second prediction frame; and

a delta frame buffer for storing the first portion of the field and the second portion of the field.--